



Cofc

ATTORNEY'S DOCKET NO.: S1022.80707US00

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Ferruccio Frisina
Serial No.: 09/925,080 Patent No. 6,809,383 B2
Filed: August 8, 2001 Issued: October 26, 2004
For: METHOD OF MANUFACTURING AN INTEGRATED EDGE STRUCTURE
FOR HIGH VOLTAGE SEMICONDUCTOR DEVICES, AND RELATED
INTEGRATED EDGE STRUCTURE

Examiner: Luu, Chuong A.
Art Unit: 2825 Confirmation No.: 3073

Correspondence and Mail Division
Certificate of Correction Branch
P.O. Box 1450
Alexandria, VA 22313-1450

Certificate
NOV 09 2004
of Correction

**REQUEST FOR CERTIFICATE
OF CORRECTION UNDER 37 C.F.R. §1.323**

Sir/Madam:

Patentees respectfully request the correction of an error in the above-captioned patent. Specifically, there is an error in the Related U.S. Application Data section on the title page of issued U.S. Patent No. 6,809,383 B2.

Item (62) on the title page currently reads:

Related U.S. Application Data

(62) Division of application No. 09/457,069 filed Dec. 7, 1999, now U.S. Pat. No. 6,300,171, and a division of application No. 09/703,263, filed Oct. 31, 2000 now abandoned.

In reviewing issued U.S. Patent No. 6,809,383 Patentee notes that the claim of priority to U.S. Serial No. 09/703,263, filed Oct. 31, 2000 was incorrect. This patent is not related to Serial No. 09/703,263, filed October 31, 2000 entitled "Switching Circuit", the insertion of this information was a clerical error. As indicated on the original transmittal letter, this application is a division of Serial No. 09/457,069, U.S. Patent No. 6,300,171 entitled "Method Of Manufacturing An Integrated Edge Structure For High Voltage Semiconductor Devices, And Related Integrated Edge Structure" which issued on October 9, 2001.

11/05/2004 SSESHE1 00000018 6809383

01 FC:1811

100.00 0P

NOV 17 2004



ATTORNEY'S DOCKET NO.: S1022.80707US00

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Ferruccio Frisina
Serial No.: 09/925,080 Patent No. 6,809,383 B2
Filed: August 8, 2001 Issued: October 26, 2004
For: METHOD OF MANUFACTURING AN INTEGRATED EDGE STRUCTURE
FOR HIGH VOLTAGE SEMICONDUCTOR DEVICES, AND RELATED
INTEGRATED EDGE STRUCTURE

Examiner: Luu, Chuong A.
Art Unit: 2825

Confirmation No.: 3073

Correspondence and Mail Division
Certificate of Correction Branch
P.O. Box 1450
Alexandria, VA 22313-1450

Sir/Madam:

Transmitted herewith for filing is/are the following document(s):

- ☒ Request for Certificate of Correction
- ☒ Copies of: Original Transmittal and title Page of U.S. 6,809,383
- ☒ PTO Form SB/44
- ☒ Return Post Card

If the enclosed papers are considered incomplete, the Mail Room and/or the Application Branch is respectfully requested to contact the undersigned collect at (617)720-3500, Boston, Massachusetts.

A check in the amount of \$100.00 is enclosed. If the check submitted is insufficient, the Commissioner is hereby authorized to charge the remaining amount to the account of the undersigned, Deposit Account No. 28/2325. A duplicate of this sheet is enclosed.

CERTIFICATE OF MAILING UNDER 37 C.F.R. §1.8(a)

I hereby certify that this document is being placed in the United States mail with first-class postage attached, addressed to Correspondence and Mail Division, Certificate of Correction Branch, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on the 2nd day of November, 2004.

Attorney Docket No.: S1022.80707US00
XNDD

Respectfully submitted,

Ferruccio Frisina, Applicant

By:
James H. Morris, Reg. No.: 34,681
WOLF, GREENFIELD & SACKS, P.C.
600 Atlantic Avenue
Boston, Massachusetts 02210
Tel. (617) 720-3500

NOV 17 2004



ATTORNEY'S DOCKET NO.: S1022.80707US00

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Ferruccio Frisina
Serial No.: 09/925,080 Patent No. 6,809,383 B2
Filed: August 8, 2001 Issued: October 26, 2004
For: METHOD OF MANUFACTURING AN INTEGRATED EDGE STRUCTURE
FOR HIGH VOLTAGE SEMICONDUCTOR DEVICES, AND RELATED
INTEGRATED EDGE STRUCTURE

Examiner: Luu, Chuong A.
Art Unit: 2825

Confirmation No.: 3073

Correspondence and Mail Division
Certificate of Correction Branch
P.O. Box 1450
Alexandria, VA 22313-1450

Sir/Madam:

Transmitted herewith for filing is/are the following document(s):

- ☒ Request for Certificate of Correction
- ☒ Copies of: Original Transmittal and title Page of U.S. 6,809,383
- ☒ PTO Form SB/44
- ☒ Return Post Card

If the enclosed papers are considered incomplete, the Mail Room and/or the Application Branch is respectfully requested to contact the undersigned collect at (617)720-3500, Boston, Massachusetts.

A check in the amount of \$100.00 is enclosed. If the check submitted is insufficient, the Commissioner is hereby authorized to charge the remaining amount to the account of the undersigned, Deposit Account No. 28/2325. A duplicate of this sheet is enclosed.

CERTIFICATE OF MAILING UNDER 37 C.F.R. §1.8(a)

I hereby certify that this document is being placed in the United States mail with first-class postage attached, addressed to Correspondence and Mail Division, Certificate of Correction Branch, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on the 2nd day of November, 2004.

Attorney Docket No.: S1022.80707US00
XNDD

Respectfully submitted,

Ferruccio Frisina, Applicant

James H. Morris, Reg. No.: 34,681
WOLF, GREENFIELD & SACKS, P.C.
600 Atlantic Avenue
Boston, Massachusetts 02210
Tel. (617) 720-3500

NOV 17 2004

Accordingly, item (62) should read:

Related U.S. Application Data

(62) Division of application No. 09/457,069 filed Dec. 7, 1999,
now U.S. Pat. No. 6,300,171.

In support of this Request Patentees enclose highlighted copies of the Original transmittal letter from the application as filed and the title page of issued U.S. Patent No. 6,809,383. Also enclosed is PTO form SB/44.

Please issue a Certificate of Correction in U.S. Letters Patent No. 6,809,383 as specified on the attached Certificate.

The correction requested does not involve change in the patent that constitutes new matter or would require reexamination. Therefore, it is respectfully requested that the correction be made and that a Certificate of Correction be issued.

The Certificate of Correction fee due under 37 CFR §1.20(a) of \$100.00 is enclosed. If his fee is insufficient, the additional fee may be charged to the account of the undersigned, Deposit Account No. 23/2825.

Should any questions arise concerning the foregoing, please contact the undersigned at the telephone number listed below.

CERTIFICATE OF MAILING UNDER 37 C.F.R. §1.8(a)

I hereby certify that this document is being placed in the United States mail with first-class postage attached, addressed to Correspondence and Mail Division, Certificate of Correction Branch, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on the 2nd day of November, 2004.



Attorney Docket No.: S1022.80707US00
XNDD

Respectfully submitted,

Ferruccio Frisina, Applicant

By: 

James H. Morris, Reg. No.: 34,681
WOLF, GREENFIELD & SACKS, P.C.
600 Atlantic Avenue
Boston, Massachusetts 02210
Tel. (617) 720-3500

NOV 17 2004



US006809383B2

(12) **United States Patent**
Frisina(10) Patent No.: **US 6,809,383 B2**
(45) Date of Patent: **Oct. 26, 2004**(54) **METHOD OF MANUFACTURING AN INTEGRATED EDGE STRUCTURE FOR HIGH VOLTAGE SEMICONDUCTOR DEVICES, AND RELATED INTEGRATED EDGE STRUCTURE**

FOREIGN PATENT DOCUMENTS

EP	0 413 256 A	2/1991
EP	0 757 382 A	2/1997
GB	2 163 597 A	2/1986

OTHER PUBLICATIONS

European Search Report from European Patent Application 98830739.3, filed Dec. 9, 1998.

(List continued on next page.)

(75) Inventor: **Ferruccio Frisina, S. Agata Li Battiatì (IT)**(73) Assignee: **STMicroelectronics S.r.l., Agrate Brianza (IT)**

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 83 days.

(21) Appl. No.: **09/925,080**(22) Filed: **Aug. 8, 2001**(65) **Prior Publication Data**

US 2001/0053589 A1 Dec. 20, 2001

Related U.S. Application Data

(62) Division of application No. 09/457,069, filed on Dec. 7, 1999, now Pat. No. 6,300,171, and a division of application No. 09/703,263, filed on Oct. 31, 2000, now abandoned.

(30) **Foreign Application Priority Data**

Dec. 9, 1998 (EP) 98830739

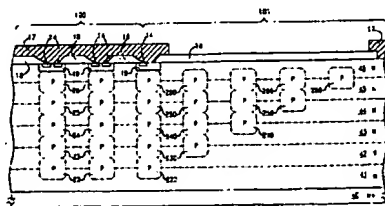
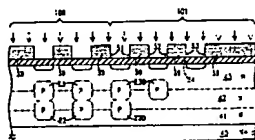
(51) Int. Cl.⁷ **H01L 29/74; H01L 23/62; H01L 29/76; H01L 29/06; H01L 21/425**(52) U.S. Cl. **257/355; 257/401; 257/409; 257/139; 257/168; 257/653**(58) Field of Search **257/341, 168, 257/409, 495, 653, 401, 342, 139, 133, 149, 147, 155, 355, 135**(56) **References Cited****U.S. PATENT DOCUMENTS**5,075,739 A * 12/1991 Davies 257/170
5,489,799 A * 2/1996 Zambrano et al. 257/587

(List continued on next page.)

Primary Examiner—Matthew Smith
Assistant Examiner—Chuong Anh Luu
 (74) *Attorney, Agent, or Firm*—Lisa K. Jorgenson; James H. Morris; Wolf, Greenfield & Sacks, P.C.

(57) **ABSTRACT**

Method of manufacturing an edge structure for a high voltage semiconductor device, including a first step of forming a first semiconductor layer of a first conductivity type, a second step of forming a first mask over the top surface of the first semiconductor layer, a third step of removing portions of the first mask in order to form at least one opening in it, a fourth step of introducing dopant of a second conductivity type in the first semiconductor layer through the at least one opening, a fifth step of completely removing the first mask and of forming a second semiconductor layer of the first conductivity type over the first semiconductor layer, a sixth step of diffusing the dopant implanted in the first semiconductor layer in order to form a doped region of the second conductivity type in the first and second semiconductor layers. The second step up to the sixth step are repeated at least one time in order to form a final edge structure including a number of superimposed semiconductor layers of the first conductivity type and at least two columns of doped regions of the second conductivity type, the columns being inserted in the number of superimposed semiconductor layers and formed by superimposition of the doped regions subsequently implanted through the mask openings, the column near the high voltage semiconductor device being deeper than the column farther from the high voltage semiconductor device.

28 Claims, 5 Drawing Sheets



UTILITY PATENT APPLICATION TRANSMITTAL <small>(Only for new nonprovisional applications under 37 CFR 1.53(b))</small>		Attorney Docket No.	S1022/8707
		First Named Inventor or Application Identifier	
		Ferruccio FRISINA	
		Express Mail Label No.	EL844519516US
		Date of Deposit	August 8, 2001
APPLICATION ELEMENTS <small>See MPEP chapter 600 concerning utility patent application contents</small>		ADDRESS TO: Box Patent Application Commissioner for Patents Washington, DC 20231	
<p>1. <input checked="" type="checkbox"/> Fee Transmittal Form <i>(Submit an original, and a duplicate for fee processing)</i></p> <p>2. <input type="checkbox"/> Applicant claims small entity status. See 37 CFR 1.27. <input type="checkbox"/> Statement filed in prior application, Status still proper and desired.</p> <p>3. <input checked="" type="checkbox"/> Specification [Total pages 11] 7 - pages description 1 - pages abstract 3 - pages claims 20 - Total claims</p> <p>4. <input checked="" type="checkbox"/> Drawing(s) (35 USC 113) [Total sheets 5] <input type="checkbox"/> Informal <input checked="" type="checkbox"/> Formal [Total drawings 12]</p> <p>5. <input checked="" type="checkbox"/> Oath or Declaration [Total pages 3] a. <input type="checkbox"/> Newly executed (original or copy) b. <input checked="" type="checkbox"/> Copy from a prior application (37 CFR 1.63(d)) <i>(for continuation/divisional with Box 17 completed)</i> <i>[Note Box 6 below]</i> i. <input type="checkbox"/> DELETION OF INVENTOR(S) Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR 1.63(d)(2) and 1.33(b).</p> <p>6. <input checked="" type="checkbox"/> Incorporation by Reference <i>(usable if Box 5b is checked)</i> The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein. See 18.</p> <p>7. Application Data Sheet, See 37 CFR 1.76</p>		<p>8. <input type="checkbox"/> CD-ROM or CD-R, in duplicate, large table or Computer Program (Appendix)</p> <p>9. <input type="checkbox"/> Nucleotide and/or Amino Acid Sequence Submission (if applicable, all necessary) a. <input type="checkbox"/> Computer Readable Form (CRF) b. <input type="checkbox"/> Specification Sequence Listing on: i. <input type="checkbox"/> CD-ROM or CD-R (2 copies); or ii. <input type="checkbox"/> paper (identical to computer copy) c. <input type="checkbox"/> Statement verifying identity of above copies</p> <p>ACCOMPANYING APPLICATION PARTS</p> <p>10. <input type="checkbox"/> Assignment Papers/cover sheet & documents(s)</p> <p>11. <input type="checkbox"/> 37 CFR 3.73(b) Statement <i>(when there is an assignee)</i> <input type="checkbox"/> Power of Attorney</p> <p>12. <input type="checkbox"/> English Translation of Document <i>(if applicable)</i></p> <p>13. <input checked="" type="checkbox"/> Information Disclosure Statement/PTO-1449 <input type="checkbox"/> Copies of IDS Citations</p> <p>14. <input type="checkbox"/> Preliminary Amendment</p> <p>15. <input checked="" type="checkbox"/> Return Receipt Postcard (MPEP 503) <i>(Should be specifically itemized)</i></p> <p>16. <input type="checkbox"/> Certified Copy of Priority Document(s) <i>(if foreign priority is claimed)</i></p> <p>17. <input type="checkbox"/> Request and Certification Under 35 U.S.C. §122(b)(2)(B)(ii)</p> <p>18. <input type="checkbox"/> Other: _____ _____ _____</p>	
19a. PURSUANT TO 35 U.S.C. §119, APPLICANT HEREBY CLAIMS PRIORITY TO EUROPEAN PATENT 98830739.3, FILED DECEMBER 9, 1998			

EL844519516US

20. If a CONTINUING APPLICATION, check appropriate box and supply the requisite information below and in the body of the application, or a preliminary amendment, or in an Application Data Sheet under 37 CFR 1.76:

☐ Continuation ☒ Divisional ☐ Continuation-in-part (CIP) of prior application No.: 09/457,069, filed on December 7, 1999, entitled METHOD OF MANUFACTURING AN INTEGRATED EDGE STRUCTURE FOR HIGH VOLTAGE SEMICONDUCTOR DEVICES, AND RELATED INTEGRATED EDGE STRUCTURE and now allowed.

☒ Cancel in this application claims 1-12 before calculating the filing fee.

☒ Amend the specification by inserting before the first line of the specification on page 1, after the title, the following:

--This application is a division of prior application No.: 09/457,069, filed on December 7, 1999, entitled METHOD OF MANUFACTURING AN INTEGRATED EDGE STRUCTURE FOR HIGH VOLTAGE SEMICONDUCTOR DEVICES, AND RELATED INTEGRATED EDGE STRUCTURE and now allowed.--

Prior application information:

Examiner Hoai V. Pham

Group Art Unit: 2814

For CONTINUATION OR DIVISIONAL APPS only: The entire disclosure of the prior application, from which an oath or declaration is supplied under Box 5b, is considered a part of the disclosure of the accompanying continuation or divisional application and is hereby incorporated by reference. The incorporation can only be relied upon when a portion has been inadvertently omitted from the submitted application parts.

18. CORRESPONDENCE ADDRESS

Correspondence address below

CUSTOMER NUMBER



23628

OR

ATTORNEY'S NAME	James H. Morris, Reg. No. 34,681				
NAME	Wolf, Greenfield & Sacks, P.C.				
ADDRESS	600 Atlantic Avenue				
CITY	Boston	STATE	MA	ZIP	02210
COUNTRY	USA	TELEPHONE	(617) 720-3500	FAX	(617) 720-2441

19. SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT REQUIRED

NAME	James H. Morris, Reg. No. 34,681
SIGNATURE	
DATE	August 8, 2001

Inventor or Identifier: Ferruccio FRISINA

Serial No: Not yet assigned

Filed: Herewith

For: METHOD OF MANUFACTURING AN INTEGRATED EDGE STRUCTURE FOR
HIGH VOLTAGE SEMICONDUCTOR DEVICES, AND RELATED INTEGRATED
EDGE STRUCTURE

CHECK BOX, if applicable:

**DUPLICATE****Fee Calculation Sheet**

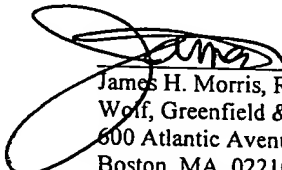
CLAIMS	FOR	NUMBER FILED	NUMBER EXTRA	RATE	FEE
	TOTAL CLAIMS (37 CFR 1.16(c))	8 - 20=	0 x	\$18	= \$ 0.00
	INDEPENDENT CLAIMS (37 CFR 1.16(b))	1 - 3=	0 x	\$80	= \$ 0.00
	MULTIPLE DEPENDENT CLAIMS (if applicable) (37 CFR 1.16(d)) +			\$260	= \$
				BASIC FEE (37 CFR 1.16(a))	\$ 710.00
	Total of above Calculations =				\$ 710.00
	Reduction by 50% for filing by small entity (Note 37 CFR 1.9, 1.27, 1.28).				\$
	Assignment Recordation Fee (if any)				\$
	Other Fees (if any).				\$
	TOTAL =				\$ 710.00

1. A check in the amount of \$ 710.00 is enclosed.

General Authorization to Charge Deposit Account and General Request for Extension of Time

2. a. ☒ If the filing of any paper in this application necessitates the payment of a fee under 37 CFR §§ ☒ 1.16 ☒ 1.17 or ☐ 1.18, and the fee due is in an amount different from any enclosed check or if no check is enclosed, the Commissioner is hereby authorized to charge any deficiency or credit any overpayment to Deposit Account No. 23/2825.
- b. ☐ The applicant hereby revokes any prior authorization to charge a fee due under 37 CFR §§ ☐ 1.16 ☐ 1.17 or ☐ 1.18.
3. If the filing of any paper in this application necessitates an extension of time under 37 CFR §1.136(a), the applicant hereby requests such extension of time. If the fee due is in an amount different from any enclosed check or if no check is enclosed, the Commissioner is hereby authorized to charge any deficiency or credit any overpayment to Deposit Account No. 23/2825.

Docket No. S1022/8707
Date: August 8, 2001


James H. Morris, Reg. No. 34,681
Wolf, Greenfield & Sacks, P.C.
600 Atlantic Avenue
Boston, MA 02210-2211
(617) 720-3500
Attorneys of Record

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : 6,809,383 *B2*
DATED : October 26, 2004
INVENTOR(S) : Ferruccio Frisina

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Item (62) on the title page should read:

Related U.S. Application Data

(62) Division of application No. 09/457,069 filed Dec. 7, 1999, now
U.S. Pat. No. 6,300,171.

MAILING ADDRESS OF SENDER

PATENT NO. 6,809,383

James H. Morris
Wolf, Greenfield & Sacks, P.C.
600 Atlantic Avenue
Boston, Massachusetts 02210

NOV 17 2004